Chapter 5: Scan Chains and Serial Testing

5.1 Introduction to Scan Chains and Serial Testing

Scan chains and serial testing are key techniques used in **Design for Testability (DFT)** that help to improve the testability of digital circuits, particularly complex integrated circuits (ICs) and systems-on-chip (SoCs). These techniques allow designers to verify the functionality of digital systems by enabling efficient and comprehensive testing of internal components that are otherwise inaccessible during regular operation.

A **scan chain** is a sequence of flip-flops or other sequential elements that are connected in series, forming a shift register. This structure allows for easy access to internal states of a system, enabling both control and observation during testing. **Serial testing** uses scan chains as part of a broader test strategy, applying test vectors in a serial manner to check the internal behavior of the system.

In this chapter, we will explore the concept of scan chains, how they are implemented, and their role in serial testing. We will also look at the benefits and challenges of using scan chains for testing digital circuits.

5.2 Concept of Scan Chains

5.2.1 What is a Scan Chain?

A **scan chain** is a series of flip-flops (or other sequential elements) that are connected together in a way that allows their states to be shifted in and out, making them accessible for testing. The scan chain is a key element in **scan-based testing**, a widely used method in DFT that improves the testability of integrated circuits by enabling access to the internal state of the system.

- **Shift Register**: In a scan chain, each flip-flop is connected in a linear fashion, and its output is connected to the input of the next flip-flop in the chain. The inputs of these flip-flops can be controlled by external test vectors, and the outputs can be observed after the test process.

- **Scan-In and Scan-Out**: The process of shifting data into and out of the scan chain is referred to as **scan-in** and **scan-out**. During testing, test data is shifted into the scan chain from the input (scan-in), and the responses from the internal nodes of the circuit are shifted out (scan-out) for comparison with the expected values.

5.2.2 How Scan Chains Work

- **Test Pattern Application**: During the testing phase, a series of test vectors are applied to the scan chain. These test patterns are used to excite the logic inside the circuit, and the responses are monitored to detect faults.

- **Scan Mode**: When the circuit enters **scan mode**, the regular data path is replaced with the scan chain. The data is shifted into the flip-flops in the scan chain, allowing them to be observed and controlled directly by the test equipment.

- **Test Data Flow**: The scan chain enables the testing process by creating a controlled, predictable flow of data that allows for easy observation of faults in sequential logic, making it especially useful for **sequential circuits** like registers and memory elements.

5.3 Role of Scan Chains in Serial Testing

Scan chains play a central role in **serial testing**, which involves applying test vectors to the system in a serial manner. This allows for effective testing of both **combinational logic** (e.g., AND, OR gates) and **sequential logic** (e.g., flip-flops, registers).

5.3.1 Fault Detection with Serial Testing

The primary goal of serial testing is to detect faults that may arise in the internal components of a digital circuit. Using scan chains:

- **Observability**: Testers can observe the internal states of the circuit through the scan-out process, allowing for real-time detection of faults, even in complex systems where the internal logic might otherwise be inaccessible.

- **Controllability**: Scan chains allow for precise control over the inputs to the flip-flops, enabling the simulation of various conditions to detect faults such as **stuck-at faults**, **transition faults**, and **delay faults**.

- **Sequential Logic Testing**: Traditional testing methods struggle to test sequential circuits thoroughly. Scan chains overcome this by directly accessing the sequential logic elements, ensuring that internal states are tested in a structured and predictable manner.

5.3.2 Fault Coverage with Scan Chains

Scan-based serial testing is known for its high fault coverage, meaning it can detect a wide range of faults in both combinational and sequential logic. Faults that scan chains help identify include:

- **Stuck-At Faults**: These are faults where a node in the circuit is stuck at either a logic high or low value, irrespective of the input. Scan chains help detect these faults by applying test patterns that stimulate each node in the system.

- **Delay Faults**: Delay faults occur when signals propagate through the circuit slower than expected, often due to poor manufacturing or material degradation. Scan chains can help identify these faults by ensuring that the circuit behaves within the required timing parameters.

- **Bridging Faults**: These occur when two or more signals are incorrectly connected. Scan chains are effective in detecting these faults by shifting the test patterns through the system and checking for unintended signal interactions.

5.4 Advantages of Scan Chains and Serial Testing

Scan chains and serial testing offer several advantages that make them essential for modern electronic system testing:

5.4.1 Simplified Access to Internal Circuitry

By creating a chain of flip-flops that can be directly accessed, scan chains provide a simple and efficient way to control and observe the internal states of a system. This is especially useful in **multi-level ICs** and **complex SoCs**, where testing all the internal components manually is impractical.

5.4.2 Comprehensive Fault Detection

Scan chains provide a high level of fault coverage by enabling tests for both **combinational** and **sequential faults**, something traditional testing methods often struggle to address. This allows for the detection of a wide variety of manufacturing defects, ensuring the reliability of the circuit.

5.4.3 Reduced Testing Time and Cost

Scan chains simplify the testing process by automating many of the steps involved in fault detection. This leads to reduced testing time and costs, particularly in high-volume manufacturing environments where testing efficiency is critical.

5.4.4 Improved Yield and Reliability

By ensuring that the internal states of the system are accessible and testable, scan chains help identify defects early in the manufacturing process. This leads to higher yield rates, fewer defects in finished products, and greater overall reliability of the final system.

5.5 Limitations of Scan Chains and Serial Testing

While scan chains and serial testing offer significant advantages, there are some limitations to consider:

5.5.1 Design Overhead

Integrating scan chains into a design requires additional components, such as **scan flip-flops** and **multiplexers**, which add to the circuit's complexity. This increases both the **area** and **power consumption** of the design, which can be a concern for systems with tight power or size constraints.

5.5.2 Testing of Analog or Mixed-Signal Systems

Scan chains and serial testing are typically used in **digital circuits**. For **analog circuits** or **mixed-signal systems** (systems that combine digital and analog components), different test strategies may be required, as scan chains are not suitable for testing analog behavior.

5.5.3 Limited Fault Coverage in Complex Systems

While scan chains provide high fault coverage, they may still miss some types of faults, especially those related to **parasitic effects** (e.g., inductance or capacitance) or those that occur in complex **multicore** systems. As systems grow in complexity, ensuring complete fault coverage may require additional testing strategies or techniques.

5.6 Conclusion

Scan chains and serial testing are fundamental tools in the design of testable digital circuits, offering efficient methods for detecting faults, verifying functionality, and improving overall product quality. By embedding scan chains into the design, engineers can access and test the internal states of a circuit, providing greater observability and controllability during the testing process. While they offer significant benefits in terms of fault coverage, testing speed, and cost reduction, challenges such as increased design complexity and limitations in testing analog circuits must be considered when implementing scan-based testing strategies. As digital circuits continue to grow in size and complexity, scan chains and serial testing will remain essential components of **Design for Testability (DFT)**, ensuring the reliability and performance of modern electronic systems.